Atty. Docket No. P-064

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Transmittal

In re application of:	Ben TANG, et al
Serial No.:	10/029,709
Filed:	12/20/2001
For:	PLL/DLL DUAL LOOP DATA SYNCHRONIZATION UTILIZING A GRANULAR FIFO LEVEL INDICATOR

Commissioner for Patents
P. O. Box: 1450
Alexandria, VA 22313–1450

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Date: November 30, 2007

Respectfully submitted,
Ben TANG, et al.

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December 3, 2007
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Benjamim TANG et al
Filed 12/20/2001
Serial Number: 10/029,709

Date: November 30, 2007
Group Art Unit 2611
Examiner: TSE, YOUNG TOI
From: Scottsdale, Arizona 85255-0155

For: **PLL/DLL DUAL LOOP DATA SYNCHRONIZATION UTILIZING A GRANULAR FIFO LEVEL INDICATOR**

AMENDMENT AND RESPONSE

Commissioner for Patents
Mail Stop: Amendment after Final Rejection
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the final Office Action dated October 1, 2007.

Amendment and Current Status of the Claims are reflected in the listing of claims which begin on page **2** of this paper.

Remarks/Arguments begin on page **8** of this paper.

Kindly amend the claims without prejudice, as follows:

Cancel claims 34 and 38-40, without prejudice.

Add claims 46 and 47.(consisting of rewritten allowed claims 39 and 40)

Note that claims 1-29 were previously canceled.

LISTING OF CLAIMS

1. (Previously canceled)
2. (Previously canceled)
3. (Previously canceled)
4. (Previously canceled)
5. (Previously canceled)
6. (Previously canceled)
7. (Previously canceled)
8. (Previously canceled)
9. (Previously canceled)
10. (Previously canceled)
11. (Previously canceled)
12. (Previously canceled)
13. (Previously canceled)
14. (Previously canceled)
15. (Previously canceled)
16. (Previously canceled)
17. (Previously canceled)
18. (Previously canceled)
19. (Previously canceled)
20. (Previously canceled)
21. (Previously canceled)
22. (Previously canceled)
23. (Previously canceled)
24. (Previously canceled)
25. (Previously canceled)

26. (Previously canceled)

27. (Previously canceled)

28. (Previously canceled)

29. (Previously canceled)

30. (Currently amended) A dual loop synchronization system comprising:

a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO configured in a feedback loop with said PFD, and receiving a local reference clock signal;

a first-in first-out (FIFO) register receiving a parallel data input;

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register;

a comparison module receiving output signals from both said write counter and said read counter to generate the fill level; and

a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL.

31. (Previously presented) A dual loop synchronization system as in claim 30, wherein said PLL is embedded within the DLL:

32. (Currently amended) A dual loop synchronization system as in claim 30, wherein said detector coupled to the output of said FIFO register for detecting the fill level of said FIFO register is a phase detector.

33. (Currently amended) A dual loop synchronization system as in claim 32, wherein said detector coupled to the output of said FIFO register for detecting the fill level of said FIFO register is a binary phase detector.

34. (Canceled)

35. (Previously presented) A dual loop synchronization system as in claim 30, wherein said PLL further comprises:

a loop filter coupled between sad PFD and said VCO.

36. (Currently amended) A dual loop synchronization system as in claim 35, wherein the loop filter coupled between ~~sad~~ said PFD and said VCO is configured as a wide bandwidth loop for suppressing VCO phase noise.

37. (Currently amended) A dual loop synchronization system as in claim 30, wherein said digital loop filter coupled between said detector and said phase shifter of said PLL to produce ~~a~~ the phase shift in said ~~PL~~ PLL is a narrow bandwidth filter.

38. (Canceled)

39. (Canceled)

40. (Canceled)

41. (Currently amended) A method for data synchronization in a plesiochronous system comprising the steps of:

receiving write data in a first-in first out (FIFO) register;

detecting the fill level of the FIFO register at the input of a delay locked loop (DLL);

providing a signal based on the detected fill level to a phase lock loop (PLL);

receiving a local reference clock signal in the PLL;

shifting the phase of the local reference clock signal in the PLL in response to the signal based on the detected fill level provided by the DLL.

42. (Currently amended) A method for data synchronization in a plesiochronous system as in claim ~~40~~ 41, further comprising:

filtering the signal based on the detected fill level in the DLL before providing it to the PLL.

43. (Currently amended) A method for data synchronization in a plesiochronous system as in claim 42, wherein the step of filtering is performed ~~with~~ in a narrow bandwidth filter.

44. (Currently amended) A method for data synchronization in a plesiochronous system as in claim ~~40~~ 41, wherein in the step of receiving ~~a~~ the local reference clock signal in the PLL, the local reference clock is received at a phase/frequency detector in the PLL and further comprising:

filtering a signal at the output of the phase/frequency detector in a loop filter; and

providing the output of the loop filter to a VCO.

45. (Previously presented) A method for data synchronization in a plesiochronous system as in claim 44, wherein the step of filtering is performed in a wide bandwidth filter.

46. (New) A dual loop synchronization system comprising:

a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO

configured in a feedback loop with said PFD, and receiving a local reference clock signal;

a first-in first-out (FIFO) register receiving a parallel data input;

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register;

a reset counter receiving input signals from both said write counter and said read counter;

a register receiving input signals from both said reset counter and said read counter to generate the fill level; and

a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL.

47. (New) A dual loop synchronization system comprising:

a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO configured in a feedback loop with said PFD, and receiving a local reference clock signal;

a first-in first-out (FIFO) register receiving a parallel data input;

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register;

a binary decoder;

a plurality of phase detectors receiving input signals from both said write counter and said read counter and providing output signals to said binary decoder to generate the fill level; and

a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL.

REMARKS

This is in response to the Office Action dated October 1, 2007. Since December 1, 2007, falls on Saturday, this Amendment filed on December 3 is filed within 2 months of the mailing date of the final action. Examiner's indication that claims 39 and 40 would be allowable if rewritten to overcome the objection(s) and to include all the limitations of the base claim and any intervening claims is noted with appreciation. Accordingly, claims 39 and 40 have been rewritten as claims 46 and 47, respectively. Each of these claims previously depended from claim 30. Thus, claim 46 includes previous claim 30 and claim 39. Claim 47 includes previous claim 30 and claim 40. New claims 46 and 47 also incorporate amendments to overcome objections.

The claim objections raised in paragraph 1 of the Office Action are believed to be overcome by the herein amendments. In short, claim 34 has been canceled, claim 37 has been amended, claim 38 has been canceled but the contents has been incorporated into claim 30 and amended to overcome objections, claims 39 and 40 have been canceled and rewritten as claims 46 and 47, claims 41 – 44 have been amended (the objection to claim 45 being believed overcome by the amendment of claim 44).

Regarding paragraph 5 of the Office Action, Applicants confirm that throughout the time period of the invention their invention was consistently commonly owned by the same assignee, to wit, Primarion, Inc.

Regarding paragraph 6 of the Office Action, Examiner has rejected claims 30-38 and 41-45 under 35USC103(a). In the rejection, Examiner applied a newly cited reference, i.e. Gu US Patent 6,901,126 in combination with Rude US Patent 6,415,006. Although Rude was previously of record, it was not relied upon and was merely listed as one of a group of patents "all related to synchronization circuits comprising elastic memories, write counters, read counters and logic circuits for comparing the phase difference of the write and read counter states". Accordingly, this is the first opportunity

that Applicants have to point out the patentably distinct features over Gu, in combination with Rude, as well as AAPA.

It is agreed with Examiner that the Gu patent discloses a dual loop (PLL and DLL) synchronization system and that some of the components used by Gu are similar to components combined by Applicants for their invention. In the nomenclature of Gu, the disclosed structure is used in the receiver of a TDM system. In this regard, a key aspect of Gu's structure (see Fig. 3 of Gu) is that phase detector 42 receives its inputs from the data recovery 40, where the early/late signals are the relationship between the received data and reference clock.

The connection of the input of phase detector 42 to the data recovery 40 is required for the problem addressed by Gu. (In this regard, Applicants disagree with Examiner's characterization of data recovery circuit 40 as including a phase detector (not shown) and phase select circuit/filter 42 as a digital loop filter. Nowhere in the specification e.g. col. 5 lines 22, 62, does the specification suggest that recovery circuit 40 includes a phase detector. Also phase select circuit/filter 42 is consistently referred to as phase select logic circuitry, e.g. col. 6 lines 14/15, 28/29, 31, col. 8 line 67, col. 9 lines 3, 7, 16/17, line 33 or as a phase select state machine 42 at col. 9, line 42.) Thus, any analogy to Applicants' invention must characterize phase select circuit 42 as the phase detector. The connection of Gu's phase detector 42 to data recovery 40 is required by Gu to recover the clock from an input data stream, using a dual loop PLL/DLL. To accomplish Gu's desired result, Gu works on synchronizing received data (i.e. recover the clock).

In contradistinction, Applicants' phase detector 518 (see FIG. 5) receives an input from the FIFO (not a data recovery module 40 as in Gu), and then provides an output to shift the phase of the local reference clock signal in the PLL. This method of shifting the phase of the local clock in response to a signal based on the detected fill level is not suggested anywhere in Gu. The structure of Gu not only lacks a FIFO register but also lacks the connection of a phase detector in the manner invented by Applicants. Simply stated, the structure of Gu cannot achieve the result of Applicants' invention as succinctly claimed in claim 41. (This is not surprising as there is no indication in Gu that

his teaching desired to achieve Applicants' result.). Applicants' invention, as recited in claim 41 claims::

> A method for data synchronization in a plesiochronous system comprising the steps of:
>
> receiving write data in a first-in first out (FIFO) register;
>
> detecting the fill level of the FIFO register at the input of a delay locked loop (DLL);
>
> providing a signal based on the detected fill level to a phase lock loop (PLL);
>
> receiving a local reference clock signal in the PLL;
>
> shifting the phase of the local reference clock signal in the PLL in response to the signal based on the detected fill level provided by the DLL. (emphasis added).

Examiner has already noted that Gu shows no FIFO registers that are an important feature of Applicants' invention. Since Gu shows no structure that would detect the fill level of a FIFO register, a fortiori, Gu's structure cannot shift the phase of the local reference signal in the PLL in response to the signal based on the detected fill level.

In order to overcome these deficiencies in the Gu reference, Examiner uses the AAPA and cites the Rude patent as a teaching of a connection between a phase detector and a FIFO register. It is noted at the outset that the AAPA and Applicants disagree with a contention that the known prior art suggests their invention. Regarding Rude, it is noted that the patent solves the synchronization problem with bit stuffing. In other words, Rude uses "STUFF/DELETE" so that his output synchronized data will match the clean read clock. In contradistinction, Applicants create a clean clock by tracking the data coming into the FIFO and using the dual loop PLL/DLL. Thus, Applicants adjust the clock generation to match the desired data rate. In short, although Applicants and Rude address a similar problem, the solutions are completely different.

Rude teaches another one of many stuff/delete techniques. Applicants' unique solution does not use stuff/delete bits, clearly an inventive alternative.

In addition to the fundamental conceptual distinctions between Applicants' invention and the teachings of Rude, Applicants also disagree with Examiner's comparison. In particular, Examiner refers to Rude's write clock 20 and read clock 22 (see FIG. 3 of Rude) as counters. Nowhere in the specification of Rude are clocks 20 and 22 described as counters. (See e. g. col. 4, line 17). The phase/frequency of the clocks is adjusted in conjunction with the stuff bits. (Col. 4 lines 17-36) As noted hereinabove, Applicants' invention solves the synchronization problem without the use of such stuff bits.

The problem with prior art systems, such as disclosed by Rude, that use stuff bits is that the dummy data can over-accumulate or under-accumulate in brief bursts of the data causing the system to fail. For example, even if the transmit frequency matches the received frequency exactly, oscillatory overfill and underfill behavior could occur. This is analogous to how a freeway suddenly loses its ability to flow traffic as the number of cars approaches capacity.

From the foregoing, it should be apparent that Applicants have invented a novel and unobvious structure, as recited in former claim 38 (now canceled and incorporated into amended claim 30), as follows:

> A dual loop synchronization system comprising:
>
> a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO configured in a feedback loop with said PFD, and receiving a local reference clock signal;
>
> a first-in first-out (FIFO) register receiving a parallel data input;
>
> a write counter receiving a write clock signal and providing an output to said FIFO register;
>
> a read counter receiving a read clock signal and providing an output to said FIFO register;

a comparison module receiving output signals from both said write counter and said read counter to generate the fill level; and

a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL. (emphasis added)

It is noted that neither Gu nor Rude disclose such a structure. Therefore, not only is the fundamental concept of Applicants' invention patentably distinct from the teachings of the prior art, but also Applicants' structure and method, as claimed, are patentably distinct.

Applicants further note that there is no way that anyone skilled in the art would have assembled the cited grouping of references (Gu, Rude, and AAPA) without having knowledge of Applicants' teachings. There can be no other reason for bringing all these references together. Although the Supreme Court has recently raised a question about the "motivation test" for assembling references to raise a question of obviousness, the assembled references cannot withstand any test. As described hereinabove, none of the references address the problem solved by Applicants with the solution claimed as Applicants' invention. When the primary reference fails to disclose Applicants invention and that invention is not disclosed in any other reference, then the claimed invention cannot be said to be obvious. The mere coincidence of similar circuit elements found in the references cannot raise a question of obviousness when the structural connection of the circuit elements, the purpose of the particular circuit connections, their coaction, the problem addressed, and the achieved result are all different from the herein claimed invention.

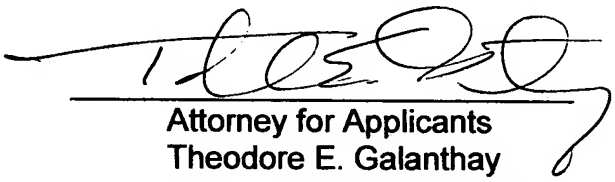
In summary, the primary reference (Gu) does not include a FIFO register; which is an important feature of Applicants' invention. To overcome this deficiency in the Gu reference, Examiner cites Rude and AAPA. However, none of the cited references teach or suggest Applicants' invention. Moreover, neither Gu nor Rude nor AAPA suggest combining the teachings of Gu with the teachings of Rude or AAPA to create

the combination of a FIFO and dual loop elements co-acting functionally to achieve the result as recited in independent claims 30 and 41.. Moreover, as noted herein, even if Gu, Rude and AAPA were combined legitimately, the combination would not result in Applicants' invention because none of the cited references addressed or solved the same problem as Applicants.

These patentable distinctions are succinctly set forth in the independent claims 30 and 41 as has been described. Claims 31 to 33 and 35-37 depend from claim 30 and are believed to be allowable for the same reasons and that they recite additional features of the invention. Claims 42-45 depend from claim 41 and are believed to be allowable for the same reasons and that they recite additional features of the invention. Claims 46 and 47 are former claims 39 and 40 rewritten in independent form and were indicated as being allowable by Examiner.

In view of the foregoing, it is believed that all the claims currently in this application are in condition for allowance. If Examiner has a question or comment or if Applicants' attorney can assist in any manner whatsoever, Examiner is respectfully requested to telephone the undersigned

Respectfully submitted,
Benjamim Tang et al



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